AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A power amplifier circuit comprising:

a first ~~amplifier configured~~ transistor coupled to an input terminal, to receive ~~an~~ a non-delayed input signal, and in response, provide ~~a first~~ an output signal;

a ~~first~~ delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first ~~amplifier~~ transistor;

a second ~~configured~~ transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal;

an impedance inverter circuit ~~configured~~ coupled to the first transistor, to provide an impedance inversion and introduce a second delay to the ~~first~~ output signal, thereby creating a second delayed output signal;

a node connecting an output of the impedance inverter circuit and an output of the second ~~amplifier~~ transistor, the node configured to combine the first and second delayed output signals, thereby creating an amplified output signal;

a level control circuit configured to provide a level control signal that causes the first ~~amplifier~~ transistor to become enabled in a low power mode, and causes the second ~~amplifier~~ transistor to become enabled in a high power mode; and

a bias control circuitry to enable the first and second ~~amplifier~~ transistors in response to the level control signal, wherein the bias control circuitry enables the first ~~amplifier~~ transistor to operate in a saturated mode when the level control signal indicates a low power mode, wherein the second ~~amplifier~~ transistor is disabled in the low power mode, and enables the second ~~amplifier~~ transistor to operate in the saturated mode when the level control signal indicates a high

power mode, wherein both the first and second ~~amplifier~~ transistors are enabled in the high power mode.

2. (Currently Amended) The power amplifier of Claim 1, wherein the bias control circuitry independently enables and disables the first and second ~~amplifier~~ transistors.

3. (Currently Amended) The power amplifier of Claim 2, wherein the bias control circuitry comprises a bias control circuit configured to generate a first bias voltage and a second bias voltage in response to ~~an analog~~ the level control signal, wherein the first bias voltage is applied to the first ~~amplifier~~ transistor and the second bias voltage is applied to the second ~~amplifier~~ transistor.

4. (Currently Amended) The power amplifier of Claim 3, wherein the bias control circuit comprises:

means for activating the first bias voltage and deactivating the second bias voltage when the ~~analog~~ level control signal identifies a low power mode; and

means for activating both the first and second bias voltages when the ~~analog~~ level control signal identifies a high power mode.

5. (Previously Presented) The power amplifier of Claim 1, wherein the level control signal is a ramp signal.

6. (Canceled)

7. (Currently Amended) The power amplifier of Claim 1, wherein ~~the first amplifier comprises a first transistor, and~~ the level control circuit comprises a first control transistor coupled between a collector of the first transistor and a voltage supply terminal.

8. (Original) The power amplifier of Claim 7, further comprising an inductor coupled between the collector of the first transistor and the first control transistor.

9. (Currently Amended) The power amplifier of Claim 7, wherein ~~the second amplifier comprises a second transistor, and~~ the level control circuit comprises a second control transistor coupled between a collector of the second transistor and the voltage supply terminal.

10. (Original) The power amplifier of Claim 9, further comprising:

an inductor coupled between the collector of the first transistor and the first control transistor; and

an inductor coupled between the collector of the second transistor and the second control transistor.

11. (Currently Amended) The power amplifier of Claim 1, wherein the ~~first~~ delay circuit comprises an inductor and one or more capacitors.

12. (Original) The power amplifier of Claim 11, wherein the impedance inverter circuit comprises an inductor and one or more capacitors.

13. (Currently Amended) The power amplifier of Claim 1, wherein the first ~~amplifier~~ transistor comprises ~~at least one~~ a heterojunction bipolar transistor, and wherein the second ~~amplifier~~ transistor comprises ~~at least one~~ a heterojunction bipolar transistor.

14. (Original) The power amplifier of Claim 1, wherein the first delay is equal to the second delay.

15. (Currently Amended) A method of amplifying an input signal, comprising:

providing the input signal to a first ~~amplifier~~ transistor in a low power mode, wherein the input signal is non-delayed;

applying a first bias voltage to a base of the first ~~amplifier~~ transistor to enable the first ~~amplifier~~ transistor in response to a level control signal;

applying a first output level control signal to a collector of the first ~~amplifier~~ transistor to cause the first ~~amplifier~~ transistor to operate in saturated mode when the first ~~amplifier~~ transistor is enabled, such that the first ~~amplifier~~ transistor provides a first output signal in response to the non-delayed input signal;

introducing a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first ~~amplifier~~ transistor;

providing the delayed input signal to a second ~~amplifier~~ transistor;

applying a second bias voltage to a base of the second ~~amplifier~~ transistor to enable the second ~~amplifier~~ transistor in response to an increase in the level control signal in a high power mode, to enable the second ~~amplifier~~ transistor to operate in a saturated mode, wherein the

second ~~amplifier~~ transistor provides a first delayed output signal in response to the delayed input signal;

introducing a second delay to the first output signal, thereby creating a second delayed output signal; and

combining the first and second delayed output signals at an output node of the second ~~amplifier~~ transistor, thereby creating an amplified output signal.

16. (Original) The method of Claim 15, further comprising selecting the first delay to be equal to the second delay, such that the first and second delayed output signals are substantially in phase.

17. (Currently Amended) The method of Claim 15, further comprising disabling the second ~~amplifier~~ transistor in a low power mode.

18. (Canceled)

19. (Previously Presented) The method of Claim 15, wherein the first output level control signal is a ramp signal.

20. (Currently Amended) The method of Claim 17, further comprising:

applying a second output level control signal to a collector of the second ~~amplifier~~ transistor.

21. (Original) The method of Claim 20, wherein the second output level control signal is a ramp signal.

22. (New) The power amplifier of Claim 1, comprising at least one first transistor and at least one second transistor.